REMARKS

Claims 1-12 are in the case and are objected to, rejected under 35 USC § 112, rejected under 35 USC § 102 over 2005/0146714 to Kitamura et al., and claim 1 is additionally rejected under 35 USC § 102 over 6,809,802 to Tsukamoto et al., 2006/0033917 to Leroux et al., 2005/0190349 to Leroux, and 2004/0126004 to Kikuchi et al. Claims 1-2 have been amended and claims 13-20 are hereby cancelled. No new matter has been introduced by the amendments, which are supported by the disclosure of the specification and figures. Reconsideration and allowance of the claims are respectfully requested.

RESTRICTION REQUIREMENT

Claims 13-20 are hereby cancelled without prejudice.

CLAIM OBJECTIONS

Claim 1 is objected to for not using a semicolon. Applicants are not aware of any law or rule that requires a semicolon to separate limitations. If the examiner is aware of any such law or rule, then applicants respectfully request that he provide a reference to such. Reconsideration and allowance are respectfully requested.

CLAIM REJECTIONS UNDER §112

Claims 1-12 are rejected for reciting "where the contours are not limited to either of the die placement boundaries and the shot placement boundaries." Applicants note that this limitation is depicted in figure 1, where the close-bounded contour lines 18a-c cross over both die placement and shot placement boundaries, and thus are not limited in placement to either of the die placement boundaries or the shot placement boundaries. Paragraph **[0020]** of the specification provides a detailed discussion of this aspect of the invention. Reconsideration and allowance of claims 1-12 are respectfully requested.

Claims 1-12 are rejected under the second paragraph for reciting the same language referenced above. Applicants assert that no essential steps have been omitted in claim 1, because the construction of close-bounded contour lines that represent integrated

circuit property information is well known in the art, such that a practitioner would not be required to perform undue experimentation in order to practice the invention.

For example, a practitioner knows where to get: (1) the plan view of the substrate, (2) the die placement boundaries, (3) the shot placement boundaries, and (4) how to construct close-bounded contour lines that represent whatever integrated circuit property he would like. Each one of these, individually, is well known in the art. All that remains is for the practitioner to then overlay this information onto a single graphical profile map as recited in claim 1. That step has never been done before this invention, and yet doing so provides startling and unexpected insight into many different kinds of yield loss issues.

The claim limitation that the contour lines are not limited to either of the die placement boundaries and the shot placement boundaries merely means that the contour lines can cross over those boundaries, and do not need to follow those boundaries. Applicants have added the words "in placement" to the claim, to make it even more clear. Thus, claims 1-12 do not omit essential steps. Reconsideration and allowance are respectfully requested.

Claims 1-12 are rejected because, it is said, it is not clear what is meant by integrated circuit property information contours. Applicants assert that this would not be unclear to a practitioner in the art, and that contour maps are well-known in a wide variety of arts and are not limited to just the integrated circuit fabrication industry. Further, the selection of properties of an integrated circuit that one might choose to depict in a contour map is endless. Reconsideration and allowance of claims 1-12 are respectfully requested.

Claims 1-12 are rejected because, it is said, the phrase "the contours are not limited to either of the die placement boundaries and shot placement boundaries" is unclear and incomplete. Specifically, the examiner asks (a) what makes the contours not limited to either of the dies placement boundaries and the shot placement boundaries, and (b) not limited in what sense? It is anticipated that the amendment as described above is sufficient to eliminate whatever concern might be left in regard to this wording. Reconsideration and allowance are respectfully requested.

Claim 2 is rejected because, it is said, it is unclear and incomplete as to what is meant by historical integrated circuit property information and how the availability is determined. Applicants again assert that this is not incomplete to a practitioner in the art. Claim 2 states that the integrated circuit property information is provided from a database of historical integrated circuit property information. Practitioners understand the concept of a database of historical information, because it is common in the industry to keep historical information on a wide range of integrated circuit properties.

The claim further states that when a ***desired amount*** of historical integrated circuit property information is available, then the database is used. A ***desired amount*** is whatever amount the practitioner ***desires*** it to be. If he desires more, then the data is not a desired amount. If he does not desire any more data, then the data is a desired amount.

The claim further states that when the desired amount of historical integrated circuit property information is not available, then the integrated circuit property information is provided by programmable algorithms. In other words, algorithms (mathematical constructs) are used to "make up" the data in any way desired. For example, data could be made up by modeling the property in question, or by modeling the process that controls the property. Data could also be made up by extrapolating or interpolating the data that is available, or by merely duplicating the available data by a factor of two or three or four or any other number. The practitioner is free to select whatever algorithm he would like to produce more data. Applicants note that such algorithms are also common in the art of data analysis, and do not intend to limit the invention to any particular method of such. "Programmable" implies that the algorithms could be implemented on a computing device. Reconsideration and allowance are respectfully requested.

Applicants note that the required level of detail in a claim is that which does not require undue experimentation by practitioners of the art. Without such a standard, the level of detail that might be insisted upon could spiral to infinity, as one put more and more information into the claim. However, if the plain meaning of the words used in the claim is understandable to a practitioner, then nothing more is needed. Applicants assert that the claims contain this level of detail.

Claim 3 is rejected because, it is said, it is unclear as to what the modification and smoothing algorithms modify and smooth. Claim 3 states that the ***programmable algorithms*** include the modification algorithms and smoothing algorithms, and claim 2 states that the ***programmable algorithms*** are applied to the integrated circuit property information. Reconsideration and allowance are respectfully requested.

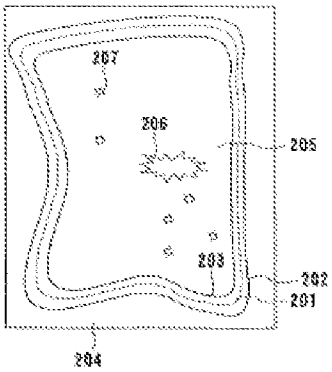
Claims 1-12 are rejected because of the effectual phrase "either A and B." Applicants used this phrase because examiners often issue rejections to any claim that contains the word "or." However, applicants have rephrased the claim in a way that the examiner might prefer. Reconsideration and allowance are respectfully requested.

CLAIM REJECTIONS UNDER §102

Independent claim 1 claims, *inter alia*, a graphical profile map for integrated circuits on a substrate, the graphical profile map comprising an overlying depiction of (1) ***die placement boundaries*** for the integrated circuits on the substrate, (2) ***shot placement boundaries*** for the integrated circuits on the substrate, and (3) ***integrated circuit property information close-bounded contour lines***, where the contour lines are not limited to either of the die placement boundaries and the shot placement boundaries (reference numbers and emphasis added).

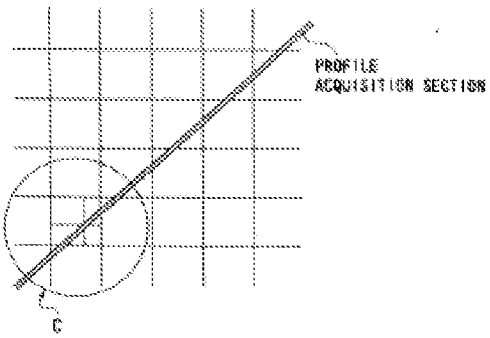
KITAMURA ET AL. do not describe such a profile map. The examiner has reference many drawings from Kitamura et al. in support of his arguments. The applicants have studied the drawings ***and the text describing the drawings*** very closely, and respectfully traverse the examiner's findings. Specifically, none of the drawings – either alone or in combination – depict, describe, or make obvious a combined map having (1) die placement boundaries, (2) shot placement boundaries, and (3) circuit property information close-bounded contour lines. In fact, none of the referenced drawings of Kitamura et al. depict either (1) die placement boundaries or (2) shot placement boundaries, which fact is revealed by reading the text that describes the drawings.

For example, figure 64 is reproduced below:



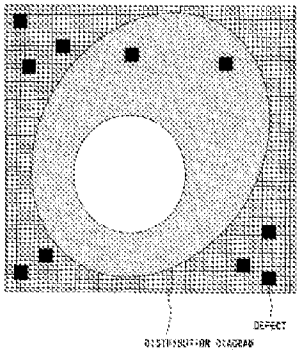
From the associated description of paragraphs 596 and 597 of Kitamura et al., we learn that line 201 is a boundary line of a pattern image to be inspected. Lines 202 and 203 are outer and inner limits, respectively, formed at a predetermined width, and which define an edge area. Element 204 is the area outside of the pattern (the grounding) and element 205 is the area inside of the pattern. Elements 207 indicate pixel clusters that are erased, and element 206 represents a pixel cluster that is flagged as a defect. Nowhere in the description of figure 64 is anything said about a die boundary or a shot boundary.

Similar deficiencies are found in all of the Kitamura et al. figures that are referenced by the examiner. None of them describe or depict (1) die placement boundaries or (2) shot placement boundaries. Figure 74 of Kimura looks like it might depict such things, but upon reading the text of Kitamura et al. that describes the figure, it is quickly learned that it does not. Figure 74 is reproduced below:



Paragraph 642 states that the double line in this figure shows the profile acquisition section, and the intersections of the grid represent positions of the pixels. The circle shows positions where the luminance value of the pattern image is acquired. Thus, this figure does not depict (1) die boundaries or (2) shot boundaries.

As a further example, figure 109 is reproduced below:

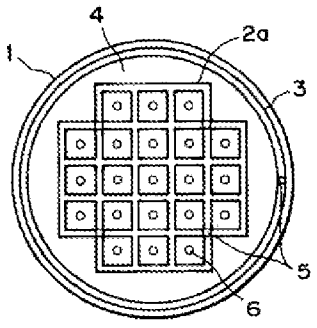


In this figure, the grid area of the image represents (as described in paragraph 842) an area of the largest deformation quantity of line width, the dotted area represents the larger deformation quantity, and the white area represents a normal deformation quantity. Again, there are no (1) die boundaries or (2) shot boundaries depicted.

Although only three specific examples of the failings of the teachings of Kitamura et al. have been given above, the other referenced figures have even more blatant failings. Thus, claim 1 patentably defines over Kitamura et al. Reconsideration and allowance of claim 1 are respectfully requested. Dependent claims 2-12 depend from independent claim 1, and contain additional important aspects of the invention, many of which are not given even the briefest mention or allusion to in Kitamura et al. Therefore, dependent claims 2-12 patentably define over Kitamura et al. Reconsideration and allowance of dependent claims 2-12 are respectfully requested.

TSUKAMOTO ET AL. also do not describe such a profile map. Figure 1A is reproduced below.

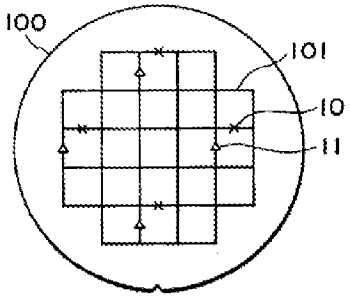
FIG. 1A



Element 1 is a wafer chuck, element 2a is a rim type protrusion, 3 is a ring type protrusion, 4 is a region between elements 2a and 3, and elements 5 and 6 are gas pressure bores in the surface of the chuck 1. Thus, figure 1A does not depict a substrate,

die or shot boundaries, or contours, all as recited in claim 1. Figure 1B is reproduced below.

FIG. 1B

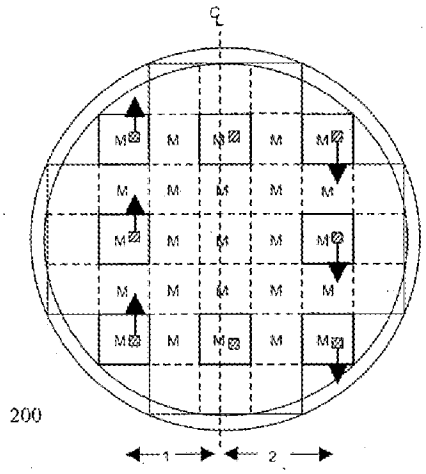


Element 100 is a substrate, elements 101 are shots, and elements 10 and 11 are locations of alignment marks. The shots 101 of figure 1B might correspond to the (2) shot boundaries as presently claimed. However, no (1) die boundaries or (3) circuit property contour lines are depicted. Figure 1C depicts only an alignment mark. Thus, the combined teachings of figure 1 do not depict the map as presently recited in claim 1.

Figures 4, 6A, and 7a also depict a wafer chuck, and thus – similar to that as described above in regard to figure 1A – do not depict any of the elements recited in claim 1. Figure 6B depicts a substrate with similar elements to those described above in regard to figure 1B, and figures 6C and 7B depict alignment marks. Thus, the combined teachings of Tsukamoto et al. do not describe the map as presently recited in claim 1.

Thus, claim 1 patentably defines over Tsukamoto et al. Reconsideration and allowance of claim 1 are respectfully requested. Dependent claims 2-12 depend from independent claim 1, and contain additional important aspects of the invention. Therefore, dependent claims 2-12 patentably define over Tsukamoto et al. Reconsideration and allowance of dependent claims 2-12 are respectfully requested.

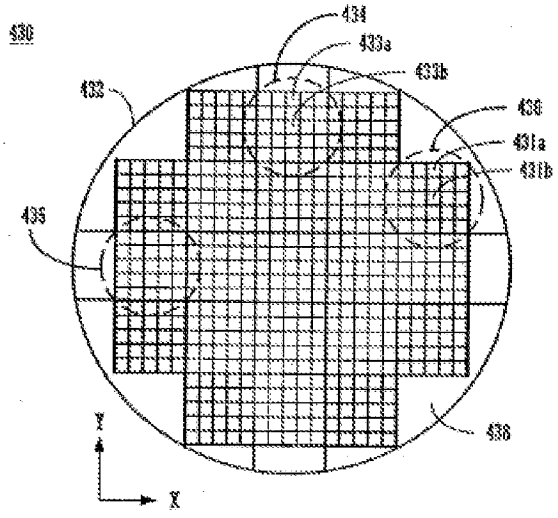
LEROUX ET AL. also do not describe such a profile map. Figures 2 and 5 are flow-charts for a method, and do not describe any one of (1) the map of the combined elements as recited in claim 1 and described at length above, (2) the construction of such a map, or (3) the use of such a map. Figure 3 is reproduced below.



Substrate 20 has been fabricated with the process outlined in figure 2. Elements M are dice and the arrows indicate offsets. It is noted that an arrow is not a close-bounded contour line. It is also noted that the dice M are indicated by the boundary lines and not by the small, hatched boxes. Thus, no (2) shot boundaries or (3) property contour lines are depicted. Figure 6 (similar to figure 3) also does not depict any (2) shot boundaries or (3) property contour lines.

Thus, claim 1 patentably defines over Leroux et al. Reconsideration and allowance of claim 1 are respectfully requested. Dependent claims 2-12 depend from independent claim 1, and contain additional important aspects of the invention. Therefore, dependent claims 2-12 patentably define over Leroux et al. Reconsideration and allowance of dependent claims 2-12 are respectfully requested.

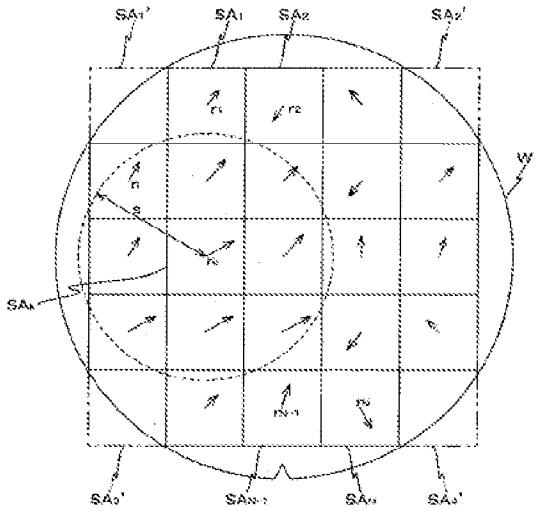
LEROUX also does not describe such a profile map. Figure 4A is a top view of a wafer with several shots and patterns, and is reproduced below.



Element 430 is a wafer with shots 434, 435, 436 and pattern boxes 433. No (3) property contour lines are depicted. Figure 5A depicts a single shot with circuits therein. Again, no (3) property contour lines are depicted.

Thus, claim 1 patentably defines over Leroux. Reconsideration and allowance of claim 1 are respectfully requested. Dependent claims 2-12 depend from independent claim 1, and contain additional important aspects of the invention. Therefore, dependent claims 2-12 patentably define over Leroux. Reconsideration and allowance of dependent claims 2-12 are respectfully requested.

KIKUCHI ET AL. also do not describe such a profile map. Figures 4-5, 13 and 16 are flow-charts and do not refer to the construction, use, or existence of a wafer map as described in claim 1. Figure 7 (similar to figures 14-15) is reproduced below.



Wafer W is depicted with shot areas SA, and vector arrows r. No (1) dice boundaries or (3) close-bounded property contours are depicted. Figure 14 depicts a wafer and shots, but no (1) dice boundaries or (3) close-bounded property contours (or vector arrows). Figure 15 shows a close-up of a portion of figure 14, depicting a shot, dice, and arrow vectors. However, neither the entire substrate nor close-bounded contour lines are depicted.

Thus, claim 1 patentably defines over Kikuchi et al. Reconsideration and allowance of claim 1 are respectfully requested. Dependent claims 2-12 depend from independent claim 1, and contain additional important aspects of the invention.

Therefore, dependent claims 2-12 patentably define over Kikuchi et al. Reconsideration and allowance of dependent claims 2-12 are respectfully requested.

COMMENTS ON REJECTIONS

Applicants do not at this time assert that they have invented any one of (1) a map of die placement boundaries on an image of a substrate, (2) a map of shot placement boundaries on an image of a substrate, or (3) a map of close-bounded contour lines on an image of a substrate. These three things might all be found in the prior art. What applicants have invented, however, is a novel and non-obvious map that combines all three of these elements.

It is well-settled, however, that "[c]ombination claims can consist of new combinations of old elements . . . for it may be that the combination of the old elements is novel and patentable." *Clearstream Wastewater Sys. v. Hydro-Action, Inc.*, 206 F.3d 1440, 1444, 54 USPQ2d 1185, 1189 (Fed. Cir. 2000); *Intel Corp. v. U.S. Int'l Trade Comm.*, 946 F.2d 821, 842, 20 USPQ2d 1161, 1179 (Fed. Cir. 1991) ("That all elements of an invention may have been old . . . is however, simply irrelevant. Virtually all inventions are combinations and virtually all are combinations of old elements.").

Thus, it might be possible to find each and every element somewhere in the prior art, such as with a key word search of a computerized database. However, doing such a search would merely yield a laundry list of the basic elements from which the various embodiments of the present invention are constructed, without any motivation to make the combinations such as are described in the claims. Thus, applicants assert that they have combined these possibly-known elements in a novel and nonobvious manner.

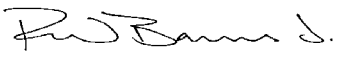
CONCLUSION

Applicants assert that the claims of the present application patentably define over the prior art made of record and not relied upon for the same reasons as given above. Applicants respectfully submit that a full and complete response to the office action is provided herein, and that the application is now fully in condition for allowance. Action in accordance therewith is respectfully requested.

In the event this response is not timely filed, applicants hereby petition for the appropriate extension of time. If any fees are required by this response, such fees may be charged to deposit account 12-2252.

Sincerely,

LUEDEKA, NEELY & GRAHAM, P.C.

By: 

Rick Barnes, 39,596

2008.01.31